Improvements in phase shifted full bridge converters.

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Abstract: *The aim of this article is to try to clarify some of the most discussed aspects of the phase shifted full bridge converter and show hidden problems:*

1. *How to extend the resonant range.*
2. *If there is a need of a capacitor in series with the transformer primary.*
3. *The placement of the current sense transformer.*

The theory was tested in a 1400W converter.

I. EXTENDING THE RESONANT RANGE.

The classic configuration of the PSFB converter is shown in fig. 1. When a MOSFET turns off, the energy in the resonant inductor Ls (which can be the primary leakage inductance) is transferred to the parasitic capacitance of the MOSFETs and this allows a smooth resonant transition in the leg. We do not try to explain more this topology as excellent full analysis is available from many sources, for example ref. [1].

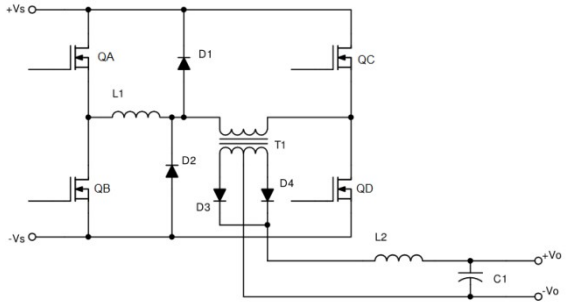

Fig. 1

A minimum current is necessary to store the necessary energy. If L1 value is too large, the maximum duty cycle is shortened. In practice it is difficult to extend the resonant range below 30% of the maximum power.

Many different ways to extend this range have been proposed, some quite complicated and using extra active switches. The following approach is based in the fact that the magnetizing current of the transformer also contributes to the resonant transition. So an air gap in the transformer can help. But the magnetizing current is proportional to the duty cycle, so the system has also a power range limit. But if an inductor in parallel with the transformer is used, the duty cycle on this inductor will be always 50% and its magnetizing current will be constant. The diagram showing this concept is shown in fig. 2.

This schematic was used in a 230V a.c. to 0-28Vd.c., 50 A, 1400 W converter that will be used as example. We found two papers based in the same principle, [2] and [3]. The later uses a transformer and the added complication perhaps does not justify the small decrease in current of the power switches.

In reference [2], R_1, R_2, R_3 and C_4 are absent, and also an equation to calculate the auxiliary inductor.

We will show that these added components are necessary for a safe operation.

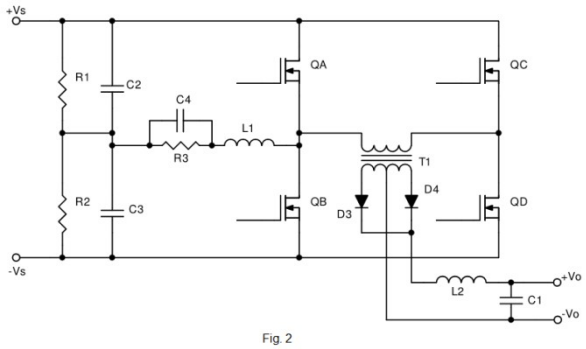

Fig. 2

Principle of operation:

Figure 2 shows the circuit connected only in the active leg (Q_A-Q_B). The passive leg (Q_C-Q_D) receives the reflected current of the output inductor, so its resonant commutation has a much more extended range. But this range can still be expanded using the proposed circuit.

During each half cycle of the converter, the voltage on L_1 goes from Vs/2 to –Vs/2. The current in L_1 swings linearly to $\pm$ ½ Vs/(2·L_1)·T/2 = Vs T/(8 L_1). When one MOSFET switches off, the current in the inductor flows to the capacitance of the MOSFETs, and the resonant transition takes place.

Because the voltage in L_1 and the time during which is applied is constant, its peak current is also constant, so if L_1 value is set correctly, the resonant transition occurs in all the power range.

Details of the circuit:

The circuit shown in [2], without R_1, R_2, R_2, C_4, has two problems. Same problems seem to happen with the circuit of ref. [3].

If the converter stops, the difference in leakage current between the MOSFETs may cause that the connecting point of C_1, C_2 diverts from Vs/2. When the inverter restarts, the current towards C_1 and C_2 increases in each pulse towards the value $Vs\sqrt{\frac{C1+C2}{L1}}$ which can be very high, the inductor can saturate and the MOSFETs be destroyed.

The solution is very simple: R_1 and R_2 drain a current much higher than the leakage current of the MOSFETs and keep the midpoint of C_1, C_2 at Vs/2 when the converter stops.

The second problem is that L_1 and C_1, C_2 form a resonant circuit, at a frequency much lower than the switching frequency. If the circuit is not dampened oscillations can be triggered and, as seen before, high peak currents may appear. An example of this is when

at low power the burst mode is active (an unavoidable feature of the UCC28950 controller).

A dampening resistor R_3 can be used. However the power dissipated in this resistor can be too high. A practical example will clarify the problem. Vs = 300 V, L_1 = 410 µH, $C_1 = C_2$ = 1 µF (200 V, ceramic), fs = 100 kHz. We can calculate ΔI_L = 1,83 A, $I_{L(RMS)}$ = 0,53 A. The ideal value of a dampening resistor (Q = 0,5) is $2 \cdot \sqrt{\frac{L1}{C1+C2}}$ = 28,6 Ω. The power in this resistor will be $28{,}6 \cdot 0{,}53^2$ W = 8 W. There are two means to reduce the power in this resistor:

1. Increase the value of C_1 and C_2. This may result in having to use electrolytics instead of ceramics. In the example, if $C_1 = C_2$ = 22 µF R_3 = 3 Ω, 0.86W.
2. Use a capacitor C_3 in parallel with R_3. C_3 has low impedance at the switching frequency but high impedance at the resonant frequency.

Calculation of the value of the auxiliary inductor

First we will show that (in spite of what is said in ref. [2]), it is not possible to use a value of L_1 such that all its energy goes to the parasitic capacitance.

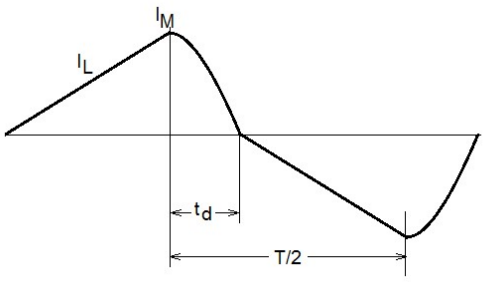

Fig. 3

Be C_p the parasitic capacitance in the node of QA source and QB drain. Assume that QA and QD are on and after half a cycle QA turns off. The current in the inductor has increased to I_M. If all the energy in the inductor goes to the capacitance:

$$½\ L_1\ I_M^2 = ½\ C_p\ V_s^2 \qquad (1)$$

The charging of C_p is done in a resonant way and the charging time is ¼ of a cycle:

$$t_d = \frac{\pi}{2}\sqrt{L_1\ C_p} \qquad (2)$$

While the mosfets are on the current increases lineally reaching the value

$$I_M = \frac{Vs\ (\frac{T}{2} - t_d)}{2\ L_1} \qquad (3)$$

Combining these three equations, the value of the inductor can be deducted:

$$L_1 = = \frac{(\frac{T}{2} - t_d)^2}{4\ C_p} \qquad (4)$$

Oddly enough, the delay time cannot be selected, it is a fixed value. If the value of L_1 is used in (2) the required value of the delay time is deducted:

$$t_d = \frac{\pi}{2(4+\pi)} T \approx 0.23\ T \qquad (5)$$

A so high value of delay time is not acceptable in a normal converter. It means that 46% of the period is lost in transitions.

This shows that the system has to be designed in a way that only a small part of the energy in the inductor is used for the resonant transition.

Fig. 4 shows the sequence.

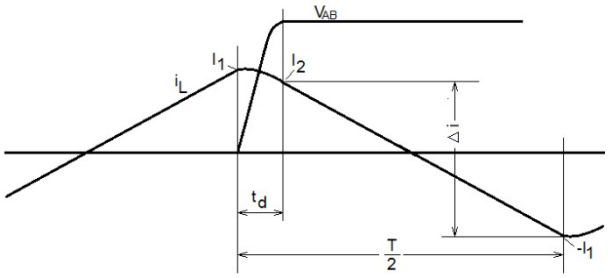

Fig. 4

The change of current in the inductor during half a cycle is

$$\Delta i = I_1 + I_2 = \frac{\frac{Vs}{2}(\frac{T}{2} - t_d)}{L_1} \qquad (5)$$

I_1 charges the capacitance and when Vs has reached its maximum value, the final current is

$$I_2 = I_1 \cdot cos\frac{t_d}{\sqrt{L_1 C_p}} \qquad (6)$$

Part of the energy in the inductor goes to the parasitic capacitance:

$$\frac{1}{2}\ (L_1(I_1^2 - I_2^2) = \frac{1}{2}\ C_p V_s^2 \qquad (7)$$

From these three equations, the following one is deducted:

$$\frac{1+\cos\frac{t_d}{\sqrt{L_1 C_p}}}{\sin\frac{t_d}{\sqrt{L_1 C_p}}} = \frac{\frac{T}{2} - t_d}{2\ L_1}\sqrt{\frac{L_1}{C_p}} \qquad (8)$$

This equation allows the calculation of L_1 from C_p, T and t_d. It has to be solved using numerical means; a hand held calculator as the HP50g will do the job. Using our 1400 W converter as an example, C_p = 740 pF, T = 10 µs, t_d = 290 ns. We get L_1 = 471 µH, I_1 = 0.8 A, I_2 = 0.7 A, I_{L1}(RMS) = 0.46 A.

Simplified equation

Because t_d << T/2, we can write:

$$\Delta i = \frac{V_S}{2\,L_1}\,\frac{T}{2};\quad I_M = \frac{\Delta i}{2} = \frac{V_S}{8}\,\frac{T}{L_1} = \frac{C_p\,V_S}{t_d}\quad ;\ \text{and}$$

$$L_1 \approx \frac{T\,t_d}{8\,C_p} \qquad (9)$$

Putting the values of C_p = 740 pF, T = 10 µs, t_d = 290 ns, we get L_1 = 490 µH which is only 4% over the exact value.

II. CAPACITOR IN SERIES WITH THE PRIMARY.

There has been quite a lot of controversy about the need of this capacitor. There is no doubt that a capacitor is series with the primary of the transformer is necessary in case of voltage control to avoid transformer saturation.

It is usually said that there is no need of such a capacitor in the case of current control. This is true in ideal operation, but there are cases were, even with current control, DC unbalance and transformer saturation can occur. Keep in mind that this kind of control measures the overall current in every leg, but not the magnetizing current.

A very small DC component can cause transformer saturation. When the power increases, the problem is worse, as the primary resistance and the MOSFET resistance decrease. In our converter the primary winding has 28 mΩ, MOSFETs have Ron = 90 mΩ (cool) and the saturation current is 1.3 A. This means that only 270 mV of DC component can cause saturation. This is less than 0.1% of the supply voltage.

Figure 5 shows a block diagram of a PSFB converter with current control. A clear case of current not being controlled is when the supply voltage (Vs) is too low and it is not possible to reach the set output voltage. Then the error amplifier (EA) saturates and current control is lost. There are two remedies to this: a capacitor in series with the primary or an under voltage lockout circuit.

An airgap in the transformer core mitigates the problem, at the expense of higher current, but does not solve it completely. The simplest and complete solution is a capacitor in series with the primary. In spite of what seems intuitive, the capacitor can be of low voltage and very small, so there is no reason to omit it and take risks.

The value of the capacitor can be calculated as following:

$$C = \frac{\frac{I_S}{N} + \frac{\Delta Is}{2\,N} + \frac{Imag}{2}}{V_c}\,t_p \qquad (10)$$

Where I_s is the secondary current, N the transformer turns ratio, Imag the peak magnetizing current, t_p the maximum pulse width and V_c the peak to peak voltage (triangular shape) in the capacitor.

In our example I_s = 25 A (current doubler, output current 50 A), ΔI_s = 3,3 A, Imag = 0,55 A, N = 3.8, t_p = 4.75 µs. Choosing Vc = 5 V it results C = 7 µF. We have used 4 x 2.2 µF ceramic capacitors, 50 V, size 1210, in parallel. If low voltage ceramic capacitors are used, their ability to withstand the RMS current has to be checked.

When using low voltage capacitors, a problem could arise when the inverter is stopped. The leakage current of the MOSFETs can cause overvoltage in the capacitor. A resistor in parallel with the capacitor (R_4 in fig. 5) solves the problem. Because the voltage in the capacitor is so low, the power in this resistor is negligible. In the converter taken as example the leakage current of the MOSFETs can reach 100 µA. We have used a 100 kΩ resistor size 0805, dissipating only 21 µW and ensuring a maximum voltage of 10 V.

III. PLACEMENT OF THE CURRENT TRANSFORMER.

If the primary current is measured with a current transformer, the usual recommended placement is shown in the position 1 of fig. 6. The main advantage is that there is no high dV/dt that causes peak currents thorough the capacitance between primary and

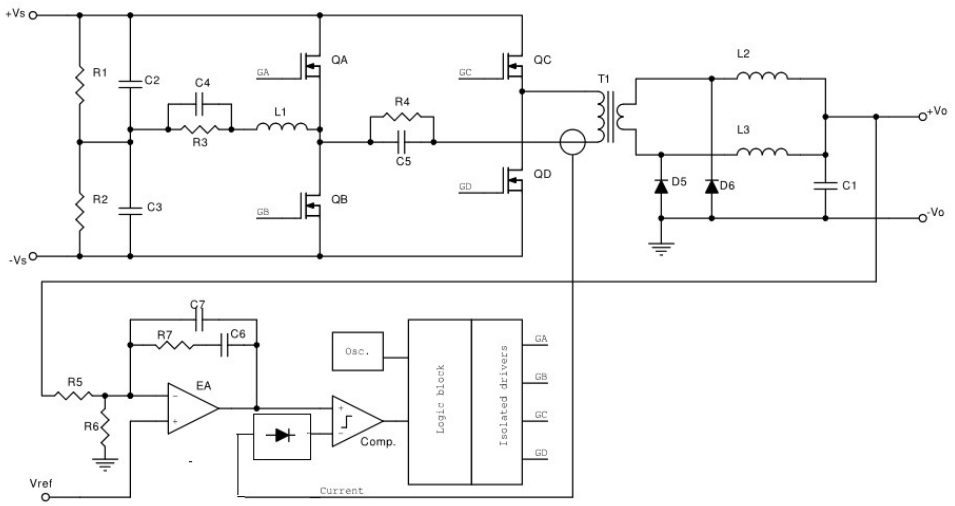

Fig. 5

secondary. But the design of the transformer is very critical. The magnetizing current has to be reset and this limits the maximum duty cycle of the converter. The secondary interwinding capacitance may be a serious problem if one wants to approach 100% duty cycle.

Using two transformers avoids these problems and allows 100% duty cycle. Each transformer has at least 50% of the cycle to reset. This approach was proposed in ref. [4]. However we cannot agree in placing the transformers in the drain of the lower MOSFETs Q_B, Q_D because of the high dV/dt there. It is better to place the transformers in the drains of Q_A, Q_C, as shown in fig. 6, position 2A and 2C.

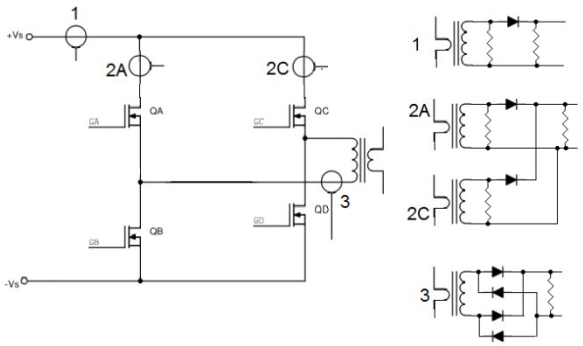

Fig. 6

If the auxiliary commutation inductor of section I is used, the current transformer placement in 1 or 2 is not convenient, because then the transformer will measure the primary current plus the current in the inductor.

Putting the transformer in series with the primary seems better: it is not affected by the peak currents between MOSFETs of the same leg and the design of the current transformer is very simple as it is well reset in spite of the interwinding capacitance and leakage inductance.

However, this placement has usually been considered a bad solution because of the two following problems:

- With synchronous rectification, in discontinuous mode current can flow from the output to the input, causing wrong measurement of current. But in any case this kind of operation has to be avoided as it can destroy the rectifying MOSFETs by overvoltage. Controllers such as the UCC28950 have ways to avoid this.

- The high dV/dt in the primary causes high peak currents through the primary to secondary capacitance. These are rectified and enter to the controller.

One solution is to put a shield between primary and secondary, connecting the shield to the secondary ground.

An easiest way is shown in fig. 7. C_1 and C_2 do the job. C_1 and C_2 form a voltage divider with the parasitic capacitance from primary to secondary. The maximum value of these capacitors is $C \leq t_d / R1$, where t_d is the admissible delay.

In our converter the transformer has a parasitic capacitance of 40 pF. With $C_1 = C_2 = 2{,}2$ nF, the parasitic pulses disappear completely. The added delay was only about 100 ns.

Saturation of the current transformer

Oddly enough, the current transformer in the primary could have a DC component. This is not likely to occur and looks as an extreme case, but it has to be taken into account.

Suppose that the bridge rectifier in fig. 7 is made of 4 discrete diodes, for example BAS16. If it happens that two of the diodes belong to a different batch, the forward voltage difference can reach 130 mV, so 260 mV for two diodes in series. But because of the maximum duty cycle is 50%, the maximum average voltage is 130 mV. The secondary will be submitted to an offset average current = 130 mV / Rs, where Rs is the resistance of the secondary. This current may saturate the transformer. Adding the small value resistor R2 will solve the problem, even if as said before is very unlikely to occur. Note that the resistor will increase slightly the secondary voltage and it has to be checked that this does not cause saturation.

An example will clarify this. In our transformer, Rs = 1,3 Ω. Isat = 70 mA, 130 mV/1,3 Ω = 100 mA, so the transformer could saturate. $R_2 = 2{,}2$ Ω solved the problem.

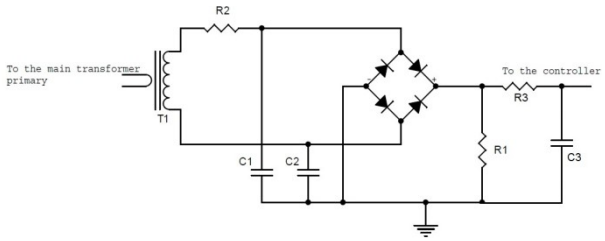

Fig. 7

Fig. 8 shows the 1400 W converter taken as example. The power semiconductors are placed on an aluminium board over the heat sink.

Fig. 8

REFERENCES:

[1] “Design of phase shifted full-bridge converter with current doubler rectifier”
Sam Abdel-Rahman
Infineon design note 2013-01, V1.0, January 2013.
[2] “A New Full Bridge Zero Switched Phase Shifted DC-DC Converter with Enlarged Duty Cycle and ZVS range”
Joao Pedro Beirante and Beatriz Vieira Borges.
Escola Superior de Tecnologia de Setubal, Portugal. 1998?
[3] “Phase_Schifted Full Bridge Converter featuring ZVS over the Full Load Range”
Bingjiang Yang, Jorge L.Duarte.
IECON 2010 – 36th Annual Conference on IEEE Industrial Electronics Society.
[4] Intersil application note 1603.
Richard Garcia. June 2011.